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TRANSMITTAL FORM <i>(to be used for all correspondence during pendency of filed application)</i>	0001/PTO Rev. 10/95	U.S. Department of Commerce Patent and Trademark Office	Application Number	09/872,435
			Filing Date	June 1, 2001
			First Named Inventor	Stephen L. Bade
			Group Art Unit Number	2123
			Examiner Name	Not yet known
Total Number of Pages in This Submission	*5	Attorney Docket Number	22178-05012	

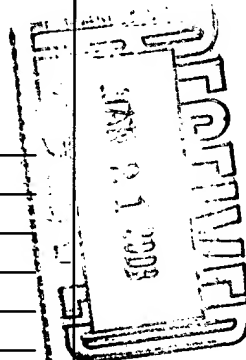
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REMARKS: *Total pages does not include total pages of cited references

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SIGNATURE OF ATTORNEY OR AGENT	
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Attorney/Reg. No.:	Edward A. Van Gieson / Reg. No.: 44,386
Dated:	11/19/02

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22178/05012/DOCS/1311359.1



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Stephen L. Bade, Shay Ben-Chorin, Paul Caamano, Marcelo E. Montoreano, Ani Taggu, Filip C. Thoen and Dean C. Wills

APPLICATION NO.: 09/872,435

FILING DATE: June 1, 2001

TITLE: Method And System For Virtual Prototyping

EXAMINER: Not yet known

GROUP ART UNIT: 2123

ATTY. DKT. NO.: 22178-05012

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INFORMATION DISCLOSURE STATEMENT

Under 37 CFR §§ 1.56 and 1.97-98

SIR:

Pursuant to the provisions of 37 CFR §§ 1.56 and 1.97-98, enclosed herewith is modified form PTO-1449/PTO-8A listing references for consideration by the Examiner. Enclosed is a copy of each listed reference that may be material to the examination of this application, and for which there may be a duty to disclose.

The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of references, or that inclusion of a reference in this list is an admission that it is prior art or is pertinent to this application, or that a search has been made, or as an admission that the information listed is, or may be considered to be, material to patentability, or that no other material information exists, and shall not be construed as an admission against interest in any manner.

This Information Disclosure Statement is being filed:

- ☐ within three months of the filing date of the application, or date of entry into the national stage of an international application, or before the mailing date of a first office action on the merits, whichever event last occurred;

- ☐ before the mailing of a first official action after the filing of a request for continued examination (RCE) under 37 CFR § 1.114;
- ☐ after three months of the filing date of this national application or the date of entry of the national stage in an international application, or after the mailing date of the first official action on the merits, whichever event last occurred, but before the mailing date of the first to occur of either: (1) a final action under 37 CFR § 1.113; or (2) an action that otherwise closes prosecution in the application, and:
 - ☐ attached hereto is the fee set forth under 37 CFR § 1.17(p) for submission of this Information Disclosure Statement under 37 CFR § 1.97(c); OR
 - ☒ Applicant certifies pursuant to 37 CFR § 1.97(e) that:
 - ☒ each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; OR
 - ☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual designated under 37 CFR § 1.56(c) more than three months prior to the filing of this Statement;
- ☐ on or before the payment of the issue fee but after the mailing date of the first to occur of either: (1) a final action under 37 CFR § 1.113; or (2) an action that otherwise closes prosecution in the application, and:
 - ☐ Applicant certifies pursuant to 37 CFR § 1.97(e) that:
 - ☐ each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; or
 - ☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a


foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual designated under 37 CFR § 1.56(c) more than three months prior to the filing of this Statement; AND

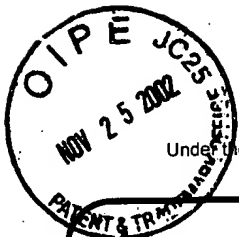
- ☐ attached hereto is the fee set forth under 37 CFR §1.17(p) for submission of this Information Disclosure Statement under 37 CFR. § 1.97(c); OR
- ☐ after the payment of the issue fee. Applicant requests that the information contained in this Information Disclosure Statement be placed in the file according to 37 CFR § 1.97(i), although the information may not be considered by the USPTO.
- ☐ This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior application No. [APPLICATION NUMBER], filed on [FILING DATE], and the references cited therein are hereby referenced, but are not required to be provided in this application under 37 CFR § 1.98(d).
- ☐ Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not received by any individual designated in 37 CFR § 1.56(c) more than thirty days prior to the filing of this Information Disclosure Statement. 37 CFR § 1.704(d).
- ☐ Applicant submits that no fee is required for the consideration of this Information Disclosure Statement.

Consideration of the listed references and favorable action are solicited.

Respectfully submitted,
STEPHEN L. BADE, SHAY BEN-CHORIN,
PAUL CAAMANO, MARCELO E.
MONTOREANO, ANI TAGGU, FILIP C. THOEN
AND DEAN C. WILLS

Dated: November 19, 2002

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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT****Complete if Known**

Application N .	09/872,435
Filing Date	June 1, 2001
First Named Inventor	Stephen L. Bade
Art Unit	2123
Examiner Name	Not yet known
Attorney Docket Number	22178-05012

Sheet	1	of	1
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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document No. Number - Kind Code ² (if known)	Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		US-		
		US-		
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A	EP 0 772 140 A	05/07/1997	Karl Van Rompaey et al.
	B	EP 0867 820 A2	09/30/1998	Patrick Schaumont et al.

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OTHER REFERENCES - NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ⁶
	C	"Co-Verification Tools: A Market Focus"; Daya Nadamuni; Embedded Systems, Programming; Sept. 1999; Miller Freeman, USA; Vol. 12, No. 9; XP-001115094; ISSN: 1040-3272; Page 119-122.	
	D	"Target Processor And Co-Verification Environment Independent Adapter-A Technology To Shorten Cycle-Time For Retargeting TI Processor Simulators In HW/SW Co-Verification Environments"; Rajesh Shah, Ramesh SubbaRa; Software Development Systems, Texas Instruments, India; ASIC/SOC Conference 1999. Proceedings Twelfth Annual IEEE; International Washington, DC USA Sept. 15-18, 1999, Piscataway, NJ, USA, IEEE, US; Sept. 15 1999; (1999-09-15); XP010360279A; ISBN: 0-7803-5632-2; pages 37-41.	
	E	"A Top-Down Hardware/Software Co-Simulation Method For Embedded Systems Based Upon A Component Logical Bus Architecture"; Mitsuhiro Yasuda, Katsuhiko Seo, Hisao Koizumi, Mitsubishi Electric Corporation, Yokohama 220-81 Japan; Barry Shackelford, Hewlett-Packard Laboratories, Palo Alto, California 94304; Fumio Suzuki, Mitsubishi Electric Corporation, Amagasaki 661 Japan; Design Automation Conference. Proceedings of the ASP-DAC Asia And South Pacific; February 10, 1998 (1998-02-10); IEEE; XP002169112A; pages 169-175.	
	F	"Hardware/Software Co-Verification, An IP Vendors Viewpoint"; Tim Hopes, EDA Engineering Manager, ARM Ltd.; Computer Design: VLSI In Computers And Processors, 1998. ICCD '98. Proceedings. International Conference on Austin, TX, USA 5-7 Oct. 1998, Los Alamitos, California, USA, IEEE Comput. Soc., U.S.; October 5, 1998 (1998-10-05), XP010310269A; ISBN: 0-8186-9099-2; pages 242-246	

Examiner Signature	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609.

Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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